REMARKS

Status of the Application

Claims 1-5 are pending. Claims 20 and 23 were objected to for informalities. Claims 1, 3, 4, 5 were rejected under 35 USC 103(a) as being unpatentable over Shiragaki (US Publication No. 2002/0162045) in view of Pierson Jr. (US 6,633,566). Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Shiragaki in view of Pierson Jr. as applied to claim 1, and further in view of Conoscenti et al. (US 5,627,836).

No amendment to the claims or the specification is made in this response. Consideration of the following remarks is requested.

Claim Rejections- 35 U.S.C. 103(a)

Claims 1, 3, 4, 5 were rejected under 35 USC 103(a) as being unpatentable over Shiragaki (US Publication No. 2002/0162045) in view of Pierson Jr. (US 6,633,566).

Applicants respectfully traverse the rejections for reasons discussed below.

Shiragaki does not disclose that "fourth, a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering the trouble" as recited in claim 1.

The Office Action indicated that "i.e. according to [0186], layer A remains in the failed state since it is not yet able to recover the failure". The applicants respectfully disagree.

According to [0014] of Shiragaki, "if a failure occurs in the system and if the failure is detected by the communication path failure reception unit 1221, which layer and which auxiliary paths will be used for failure recovery is calculated and selected in the communication path recovery target selection unit 1222...", and according to [0015], "with the configuration as described above, if the multiple layers had a failure recovery function, coordinated operation of failure recovery could be performed". It can be seen that Shiragaki seeks to resolve the problem of delay resulted by selecting one layer used for failure recovery.

According to [177] and [220] of Shiragaki:

"[177] When the failure is detected in only one layer, the failure recovery is performed in that layer only; however, a case where failure are detected in both layers will be examined below."

"[220] if the failure cannot be recovered in the layer, performing the failure recovery in the other layer, or by starting failure recovery immediately after each layer has detected the failure, and adjusting subsequently...".

It can be seen that [178-188] provide an embodiment about failure recovery when both layers detect the same failure, namely layer A and layer B detect the same failure, but not layer A detects a failure and layer B detects a different failure.

Therefore, according to [0186], it cannot be concluded directly and undoubtedly that layer A remains in the failed state based on that layer A stops failure recovery operation at that stage. The failure may occur in other layer, and layer A just stops failure recovery, which does not mean that the layer A itself encounters a failure.

The office Action asserted that "in summary a bypass is set up after layer B detects layer encountering a failure after receiving notice 203 and 208 to carry out the main signal while layer A remains in a failed state". The applicants respectfully disagree. This conclusion cannot be obtained directly and undoubtedly. Firstly, layer B cannot be informed that layer A remains in a failed state after receiving notice 203 and 208, what layer B can be informed is that layer A has started failure recovery and layer B can switch the main signal. The layer B cannot be informed whether layer A encounters a failure or not. Secondly, that a bypass is set up cannot be concluded. Layer A just stops failure recovery, which does not mean that layer A has encountered a failure. Layer A still may communicate with other layer. Though layer B can switch the main signal to complete the failure recovery, the person ordinary skill in the art cannot conclude that layer A is isolated and bypassed.

Pierson was cited to teach that "second, high layer processing module of the multi-layer communication equipment extract and insert high layer service of the said node from low layer transmission passage, avoiding changing the service between upstream node and downstream node after passing high layer processing module of the multi-layer communication equipment" as recited in claim 1. However, Pierson fails to teach such features too. Therefore, Pierson cannot cure the deficiencies of Shiragaki.

Pierson's technical solution is related to data transmission between two networks, namely ATM and SONET. For example, according to column 10 lines 14-26, the path of the data is ATM transmitter → SONET transmitter → ATM switch → SONET receiver → ATM receiver. The technical solution of claim 1 is related to data transmission between high layer processing

module and low layer processing module of one multi-layer communication equipment. The high layer processing module extracts and inserts high layer service of the said node from low layer transmission so that the service between the upstream node and downstream node of the multi-layer communication equipment can keep unchanged.

For the reasons discussed above, claim 1 is patentable over Shiragaki and Pierson. Claims 3-5 depend from claim 1 and, thus, are also patentable over Shiragaki and Pierson for at least the same reasons.

Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Shiragaki in view of Pierson Jr. as applied to claim 1, and further in view of Conoscenti et al. (US 5,627,836).

The Conoscenti was cited to teach that "a transparent virtual path connection is set up for the service passing the high layer processing module of the said node, namely for ATM, a cross connection, which changes neither virtual path identification nor virtual channel identification, will be set up, to avoid changing the service between upstream node and downstream node after passing high layer processing module of the said node" as recited in claim 2.

However, Conoscenti cannot cure the deficiencies of Shiragaki and Pierson as discussed in connection with claim 1. Therefore, claim 1 is patentable over Shiragaki, Pierson, and Conoscenti. Claim 2 depends on claim 1 and, thus, is also patentable over Shiragaki, Pierson, and Conoscenti for at least the same reasons discussed above.

Further more, Conoscenti does not specifically teach the above features recited in claim 2. Conoscenti discloses that "the cells pass through the ATM processing elements of the network without changing the VPI/VCI values" (see column 4, lines 46-62). It can be seen that the VPI/VCI values remain constant throughout the network. In the technical solution of claim 2, the VPI/VCI remains unchanged when a transparent virtual path connection is set up for the service passing the high layer processing module of the said node. That is to say, the VPI/VCI remains unchanged under special condition but does not remain unchanged throughout the network. It is not obvious for the person skill in the art to obtain the technical solution of claim 2 combining what Shiragaki, Pierson and Conoscenti disclose.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that claims 1-

5 are patentable over the cited references. Allowance of this application is earnestly solicited.

Respectively submitted
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